the respective operation modes. WC0 to WC2 are word counters and are employed to generate a display address. The bit numbers of the address are not necessarily consecutive. This is because the bits are to be commonly used in the respective operation modes so as to configure the circuit of the multiplexer **2003** as simple as possible.

As described above, according to the present invention, the data bus width of the memory can be minimized, and hence the size of the graphic processing apparatus can be reduced.

We claim:

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1. A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address in said memory means for retrieval of data from the memory locations at the different column addresses within the specified row of memory locations and processing of the retrieved data to generate graphic signals;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is an integer and $n>m$;

said memory control means including storage means for temporarily storing data received serially on said memory data bus from memory locations at different column addresses of the memory means row corresponding with the specified row address, and transmitting the temporarily stored data in parallel on said processor data bus to said data processing means for processing thereof to generate graphic signals.

2. A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address in said memory means for writing of data in the memory locations at the different column addresses within the specified row of memory locations;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is an integer and $n>m$;

said memory control means including multiplexer means for multiplexing data received in parallel on said processor data bus into serial data and applying the serial data to said memory data bus for writing thereof in memory locations at different column addresses of the memory means row corresponding with the specified row address.

3. A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address of memory locations in said memory means for transfer of a data word therewith;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is a multiple of m;

said memory control means including counter means, responsive to receipt on said processor data bus of a row address specified by said processor means to specify an n-bit data word in said memory means, for successively generating n column addresses, applying the received row address and m of the generated column addresses on said memory data bus to transfer data between said memory means and said data processor means, with the data transfer including transfer of m bits of data in parallel between said memory means and said memory control means, and transfer of n bits of data between said memory control means and said data processor means.

4. A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing pixel information;

data processing means for specifying addresses of memory locations in said memory means for retrieval of pixel information therefrom and processing of the retrieved pixel information to generate graphic signals;

memory control means coupled to said memory means an said data processing means for retrieving pixel information from said memory means and applying the retrieved pixel information to said data processing means for processing thereof; and

output means connected to said memory control means for outputting processed pixel information to generate graphics.

5. A graphic processing apparatus as claimed in claim , wherein the pixel information comprises multi-bit ixel information units corresponding to one pixel.

6. A graphic processing apparatus as claimed in claim , wherein the pixel information comprises pixel infor- ıation units, and wherein said memory control means ıcludes means for selecting the number of bits in each ixel information unit.

7. A graphic processing apparatus as claimed in claim , wherein said memory control means includes storage ıeans for temporarily storing pixel information re- ieved from said memory means.

8. A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address in said memory means for transfer of data between the data processing means and the memory loca-

tions at the different column addresses within th specified row of memory locations;

memory control means;

a memory data bus having m lines and interconnect ing the memory means and the memory contro means to transmit m bits of data in parallel therebe tween, where m is an integer; and

a processor data bus having n lines and interconnect ing the data processing means and the memor control means to transmit n bits of data in paralle therebetween, where n is an integer and $n > m$;

said memory control means including storage mean for temporarilty storing data received on sai

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memory bus from memory locations at different column addresses of the memory location row corresponding with the specified row address and transmitting the temporarily stored data in parallel on said processor data bus to said data processing means for processing thereof, and multiplexer means for multiplexing data received in parallel on said processor data bus into serial data and applying the serial data to said serial memory data bus for writing thereof in memory locations at different column addresses of the memory location row corresponding with the specified row address.